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1 Neon: a single-chip 3D workstation graphics accelerator

Joel McCormack, Robert McNamara, Christopher Gianos, Larry Seiler, Norman P. Jouppi, Ken Correll

August 1998 **Proceedings of the ACM SIGGRAPH/EUROGRAPHICS workshop on Graphics hardware**

Full text available: pdf(1.58 MB) Additional Information: full citation, references, citings, index terms

Keywords: chunk rendering, direct rendering, graphics pipeline, level of detail, rasterization, texture cache, tile rendering

2 A parallel embedded-processor architecture for ATM reassembly

Richard F. Hobson, P. S. Wong

February 1999 **IEEE/ACM Transactions on Networking (TON)**, Volume 7 Issue 1

Full text available: pdf(331.21 KB) Additional Information: full citation, references, citings, index terms

Keywords: ATM, embedded systems, medium access control, segmentation and reassembly

3 A dynamic-SDRAM-mode-control scheme for low-power systems with a 32-bit RISC CPU

Seiji Miura, Kazushige Ayukawa, Takao Watanabe

August 2001 **Proceedings of the 2001 international symposium on Low power electronics and design**

Full text available: pdf(955.52 KB) Additional Information: full citation, references, citings, index terms

Keywords: SDRAM controller, active-standby mode, standby mode

4 A performance comparison of contemporary DRAM architectures

Vinodh Cuppu, Bruce Jacob, Brian Davis, Trevor Mudge

May 1999 **ACM SIGARCH Computer Architecture News , Proceedings of the 26th annual international symposium on Computer architecture**, Volume 27 Issue 2

Full text available: pdf(166.88 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

In response to the growing gap between memory access time and processor speed, DRAM manufacturers have created several new DRAM architectures. This paper presents a simulation-based performance study of a representative group, each evaluated in a small system organization. These small-system organizations correspond to workstation-class computers and use on the order of 10 DRAM chips. The study covers Fast Page Mode, Extended Data Out, Synchronous, Enhanced Synchronous, Synchronous Link, Rambus, ...

5 Array allocation taking into account SDRAM characteristics

Hong-Kai Chang, Youn-Long Lin

January 2000 **Proceedings of the 2000 conference on Asia South Pacific design automation**

Full text available: pdf(95.08 KB) Additional Information: full citation, references, citings

6 Design space exploration for embedded systems: Energy exploration and reduction of SDRAM memory systems

Yongsoo Joo, Yongseok Choi, Hojun Shim, Hyung Gyu Lee, Kwanho Kim, Naehyuck Chang

June 2002 **Proceedings of the 39th conference on Design automation**

Full text available: pdf(196.08 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper, we introduce a precise energy characterization of SDRAM main memory systems and explore the amount of energy associated with design parameters, leading to energy reduction techniques that we are able to recommend for practical use.We build an in-house energy simulator for SDRAM main memory systems based on cycle-accurate energy measurement and state-machine-based characterizations which independently characterize dynamic and static energy. We explore energy behavior of the memory ...

Keywords: SDRAM, low power, memory system

7 Low-energy off-chip SDRAM memory systems for embedded applications

Hojun Shim, Yongsoo Joo, Yongseok Choi, Hyung Gyu Lee, Naehyuck Chang

February 2003 **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 2 Issue 1

Full text available: pdf(3.98 MB) Additional Information: full citation, abstract, references, index terms

Memory systems are dominant energy consumers, and thus many energy reduction techniques for memory buses and devices have been proposed. For practical energy reduction practices, we have to take into account the interaction between a processor and cache memories together with application programs. Furthermore, energy characterization of memory systems must be accurate enough to justify various techniques. In this article, we build an in-house energy simulator for memory systems that is accelerat ...

Keywords: Low power, SDRAM, memory system

8 EM-Cube: an architecture for low-cost real-time volume rendering

Rändy Osborne, Hanspeter Pfister, Hugh Lauer, TakaHide Ohkami, Neil McKenzie, Sarah Gibson, Wally Hiatt

August 1997 **Proceedings of the ACM SIGGRAPH/EUROGRAPHICS workshop on**

Graphics hardware

Full text available: pdf(1.04 MB) Additional Information: full citation, references, citings, index terms

9 Hybrid volume and polygon rendering with cube hardware

Kevin Kreeger, Arie Kaufman

July 1999 **Proceedings of the ACM SIGGRAPH/EUROGRAPHICS workshop on Graphics hardware**

Full text available: pdf(1.85 MB) Additional Information: full citation, references, citings, index terms

Keywords: cube architecture, mixing polygons and volumes, ray casting, run-length-encoding, volume rendering

10 Dynamic scheduling and synchronization synthesis of concurrent digital systems under system-level constraints

Claudionor N. Coelho, Giovanni De Micheli

November 1994 **Proceedings of the 1994 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(783.93 KB) Additional Information: full citation, abstract, references, citings, index terms

We present in this paper a novel control synthesis technique for system-level specifications that are better described as a set of concurrent synchronous descriptions, their synchronizations and constraints. The proposed synthesis technique considers the degrees of freedom introduced by the concurrent models and by the environment in order to satisfy the design constraints.Synthesis is divided in two phases. In the first phase, the original specification is translated into an alg ...

11 Architecture: The architecture of the DIVA processing-in-memory chip

Jeff Draper, Jacqueline Chame, Mary Hall, Craig Steele, Tim Barrett, Jeff LaCoss, John Granacki, Jaewook Shin, Chun Chen, Chang Woo Kang, Ihn Kim, Gokhan Daglikoca

June 2002 **Proceedings of the 16th international conference on Supercomputing**

Full text available: pdf(295.98 KB) Additional Information: full citation, abstract, citings, index terms

The DIVA (Data IntensiVe Architecture) system incorporates a collection of Processing-In-Memory (PIM) chips as smart-memory co-processors to a conventional microprocessor. We have recently fabricated prototype DIVA PIMs. These chips represent the first smart-memory devices designed to support virtual addressing and capable of executing multiple threads of control. In this paper, we describe the prototype PIM architecture. We emphasize three unique features of DIVA PIMs, namely, the memory interf ...

Keywords: architecture, memory bandwidth, processing-in-memory

12 Processor-based system: Unifying memory and processor wrapper architecture in multiprocessor SoC design

Férid Gharsalli, Damien Lyonnard, Samy Meftali, Frédéric Rousseau, Ahmed A. Jerraya

October 2002 **Proceedings of the 15th international symposium on System Synthesis**

Full text available: pdf(682.89 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper, we present a new methodology for application specific multiprocessor system-on-chip design. This approach facilitates the integration of existing components with the

concept of wrapper. Wrappers allow automatic adaptation of physical interfaces to a communication network. We also give a generic architecture to produce these wrappers, either for processors or for other specific components such as memory IP. This approach has successfully been applied on a low-level image processing ...

Keywords: embedded memory, memory access, memory wrapper generation, system-on-chip

13 System level issues: Energy-aware memory allocation in heterogeneous non-volatile memory systems

Hyung Gyu Lee, Naehyuck Chang

August 2003 **Proceedings of the 2003 international symposium on Low power electronics and design**

Full text available: pdf(59.50 KB) Additional Information: full citation, abstract, references, index terms

Memory systems consume a significant portion of power in hand-held embedded systems. So far, low-power memory techniques have addressed the power consumption when the system is turned on. In this paper, we consider data retention energy during the power-off period. For this purpose, we first characterize the data retention energy and cycle-accurate active mode energy of the non-volatile memory systems. Next, we present energy-aware memory allocation for a given task set taking into account arriv ...

Keywords: low-power memory, memory allocation, non-volatile memory

14 A low-cost memory architecture for PCI-based interactive ray casting

Michael Doggett, Michael Meißner, Urs Kanus

July 1999 **Proceedings of the ACM SIGGRAPH/EUROGRAPHICS workshop on Graphics hardware**

Full text available: pdf(1.12 MB) Additional Information: full citation, references, citings, index terms

Keywords: graphics hardware, memory architecture, raycasting, volume rendering accelerator, volume visualization

15 Optimizing software performance for IP frame reassembly in an integrated architecture

Peter M. Ewert, Naraig Manjikian

September 2000 **Proceedings of the second international workshop on Software and performance**

Full text available: pdf(132.48 KB) Additional Information: full citation, references, index terms

Keywords: asynchronous transfer mode, communication processors, computer architecture, event-driven simulation, software performance

16 Session 4: Low-power color TFT LCD display for hand-held embedded systems

Inseok Choi, Hojun Shim, Naehyuck Chang

August 2002 **Proceedings of the 2002 international symposium on Low power electronics and design**

Full text available: pdf(690.68 KB) Additional Information: full citation, abstract, references, citings, index terms

An LCD (Liquid Crystal Display) is a standard display device for hand-held embedded systems. Today, color TFT (Thin-Film Transistor) LCDs are common even in cost-effective equipments. An LCD display system is composed of an LCD panel, a frame buffer memory, an LCD and frame buffer controller, and a backlight inverter and lamp. All of them are heavy power consumers, and their portion becomes much more dominant when running interactive applications. This is because interactive applications are oft ...

Keywords: LCD, embedded system, low energy, low power

17 Lightning-2: a high-performance display subsystem for PC clusters

Gordon Stoll, Matthew Eldridge, Dan Patterson, Art Webb, Steven Berman, Richard Levy, Chris Caywood, Milton Taveira, Stephen Hunt, Pat Hanrahan

August 2001 **Proceedings of the 28th annual conference on Computer graphics and interactive techniques**

Full text available: pdf(2.06 MB) Additional Information: full citation, abstract, references, citings, index terms

Clusters of PCs are increasingly popular as cost-effective platforms for supercomputer-class applications. Given recent performance improvements in graphics accelerators, clusters are similarly attractive for demanding graphics applications. We describe the design and implementation of Lightning-2, a display subsystem for such a cluster. The system scales in both the number of rendering nodes and the number of displays supported, and allows any pixel data generated from any node to be dynamic ...

Keywords: graphics hardware, graphics systems, parallel computing, rendering hardware, rendering systems

18 Polygon rendering on a stream architecture

John D. Owens, William J. Dally, Ujval J. Kapasi, Scott Rixner, Peter Mattson, Ben Mowery

August 2000 **Proceedings of the ACM SIGGRAPH/EUROGRAPHICS workshop on Graphics hardware**

Full text available: pdf(161.65 KB) Additional Information: full citation, abstract, references, citings, index terms

The use of a programmable stream architecture in polygon rendering provides a powerful mechanism to address the high performance needs of today's complex scenes as well as the need for flexibility and programmability in the polygon rendering pipeline. We describe how a polygon rendering pipeline maps into data streams and kernels that operate on streams, and how this mapping is used to implement the polgyon rendering pipeline on Imagine, a programmable stream processor. We compare our resul ...

Keywords: OpenGL, SIMD, graphics hardware, kernels, media processors, polygon rendering, stream architecture, stream processing, streams

19 MEDEA workshop: Fine-grain design space exploration for a cartographic SoC multiprocessor

Alessio Bechini, Pierfrancesco Foglia, Cosimo Antonio Prete

March 2003 **ACM SIGARCH Computer Architecture News**, Volume 31 Issue 1

Full text available: pdf(948.91 KB) Additional Information: full citation, abstract, references, index terms

Traditionally, in the field of embedded systems low power consumption and low cost have been always regarded as stringent specification constraints. In recent years, high computational power has become a fundamental requirement as well. This has been mainly determined by the introduction of new features, typical of general-purpose systems, e.g.

GUI-based interfaces. In this setting, low cost, low power consumption, significant computational power and short time-to-market are conflicting needs th ...

Keywords: SoC Multiprocessors, embedded systems, multiprocessor architecture, performance evaluation, trace-driven simulation

20 Internet nuggets

Mark Thorson

June 2001 **ACM SIGARCH Computer Architecture News**, Volume 29 Issue 3

Full text available: pdf(384.73 KB) Additional Information: full citation, abstract, index terms

This column consists of selected traffic from the comp.arch newsgroup, a forum for discussion of computer architecture on Internet---an international computer network. As always, the opinions expressed in this column are the personal views of the authors, and do not necesarily represent the institutions to which they are affiliated. Text which sets the context of a message appears in italics; this is usually text the author has quoted from earlier messages. The code-like expressions below the au ...

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